

FIG.1

SYSTEM STRUCTURE DIAGRAM OF THE PRESENT INVENTION

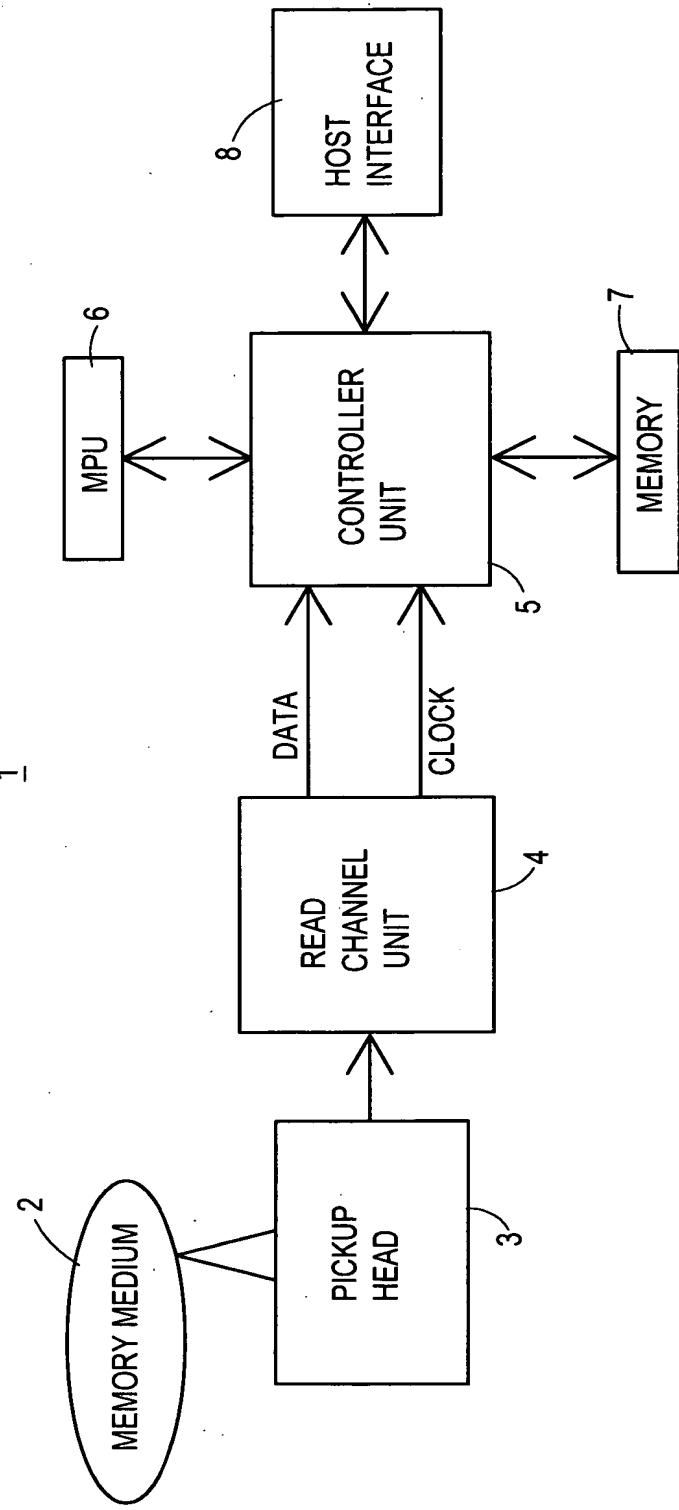


FIG.2

BLOCK DIAGRAM ILLUSTRATING A BASIC STRUCTURE OF CONTROLLER UNIT

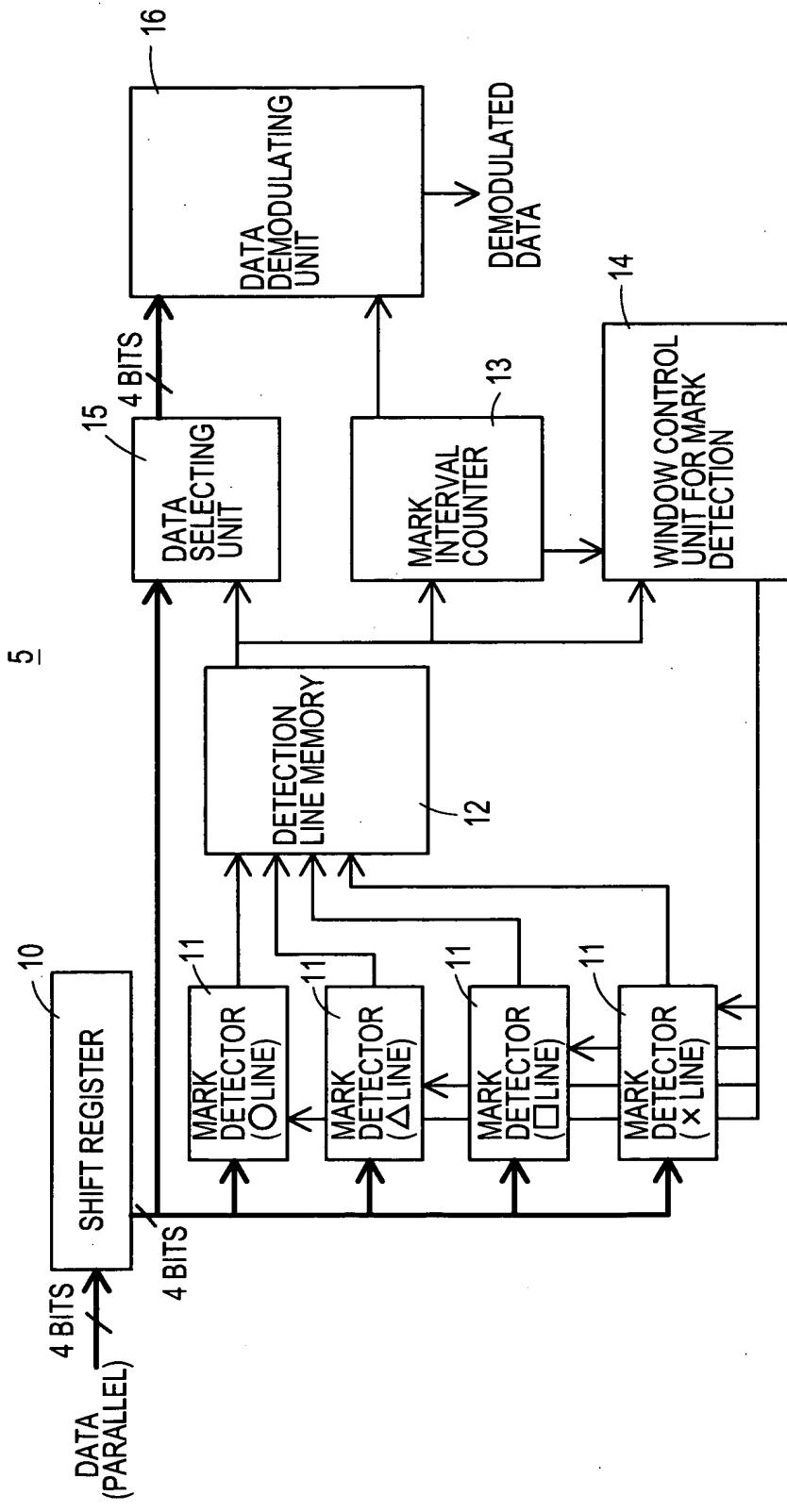


FIG.3

EXPLANATORY DIAGRAM FOR DATA DISTRIBUTION IN PARALLEL TRANSFER OF FOUR BITS

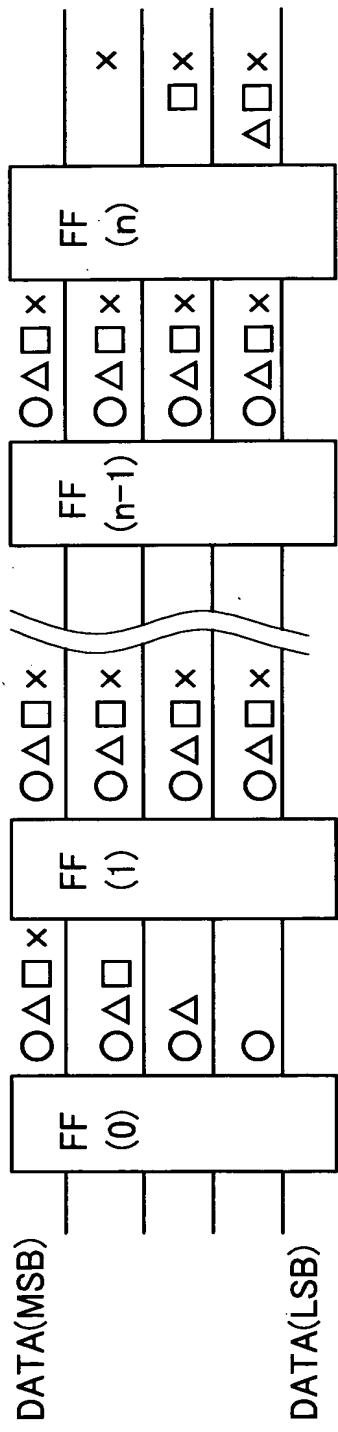


FIG.4

EXPLANATORY DIAGRAM FOR GENERATION OF MARK DETECTION WINDOW WHEN PREDETERMINED MARKS FOR DETECTING SYNCHRONIZATION ARE DETECTED IN THE O - LINE AT THE TIME OF TRANSFERRING THE DATA IN THE PARALLEL CONDITION OF FOUR BITS

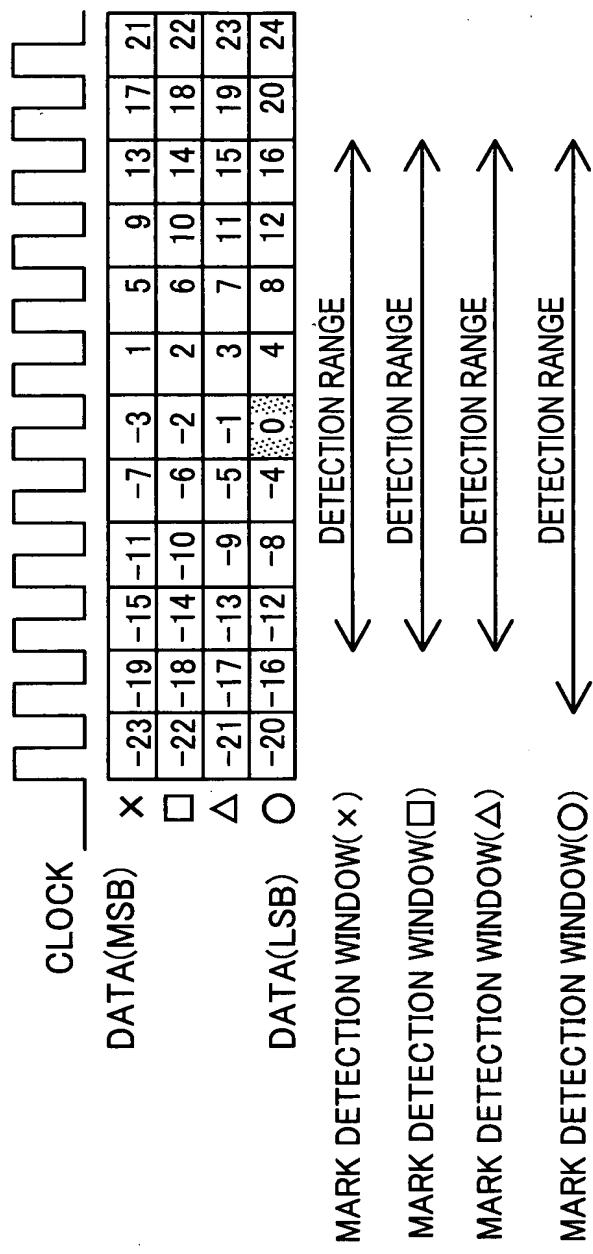


FIG.5

EXPLANATORY DIAGRAM FOR GENERATION OF MARK DETECTION WINDOW WHEN PREDETERMINED MARKS FOR DETECTING SYNCHRONIZATION ARE DETECTED IN THE Δ - LINE AT THE TIME OF TRANSFERRING THE DATA IN THE PARALLEL CONDITION OF FOUR BITS

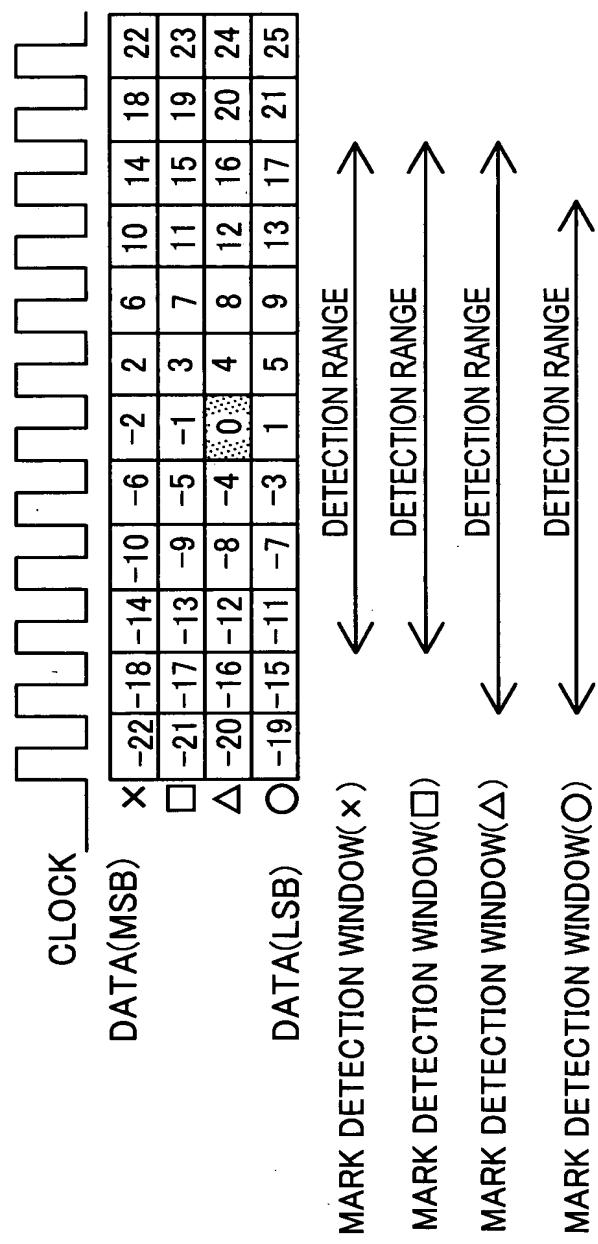


FIG.6

EXPLANATORY DIAGRAM FOR GENERATION OF MARK DETECTION WINDOW WHEN PREDETERMINED MARKS FOR DETECTING SYNCHRONIZATION ARE DETECTED IN THE □ - LINE AT THE TIME OF TRANSFERRING THE DATA IN THE PARALLEL CONDITION OF FOUR BITS

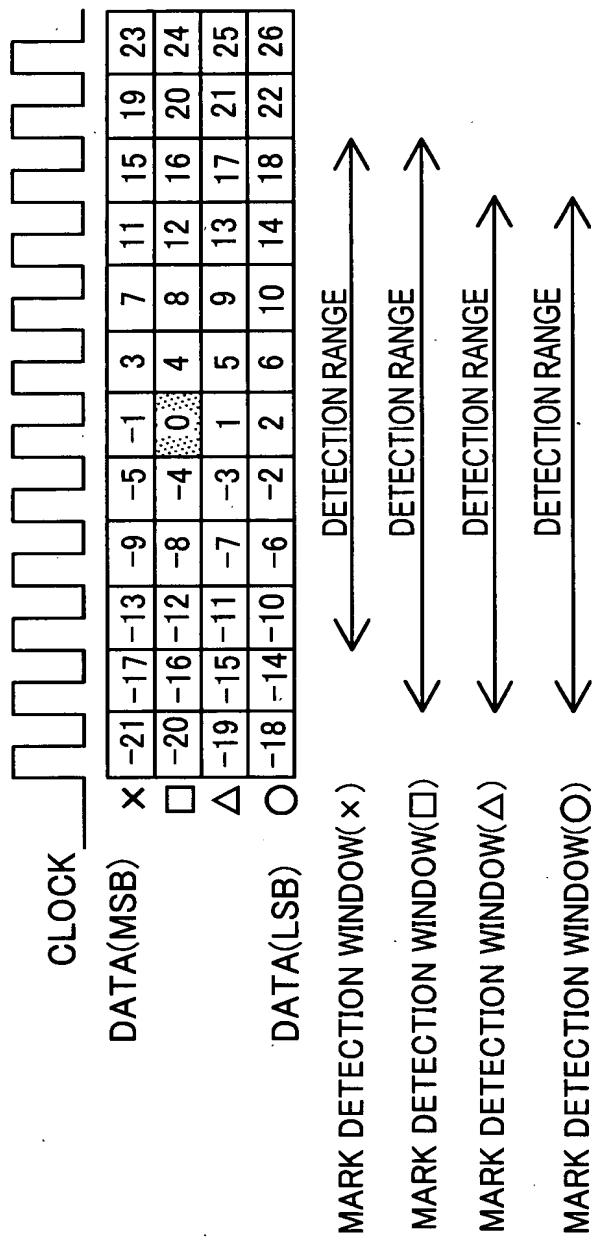


FIG.7

EXPLANATORY DIAGRAM FOR GENERATION OF MARK DETECTION WINDOW WHEN PREDETERMINED MARKS FOR DETECTING SYNCHRONIZATION ARE DETECTED IN THE X - LINE AT THE TIME OF TRANSFERRING THE DATA IN THE PARALLEL CONDITION OF FOUR BITS

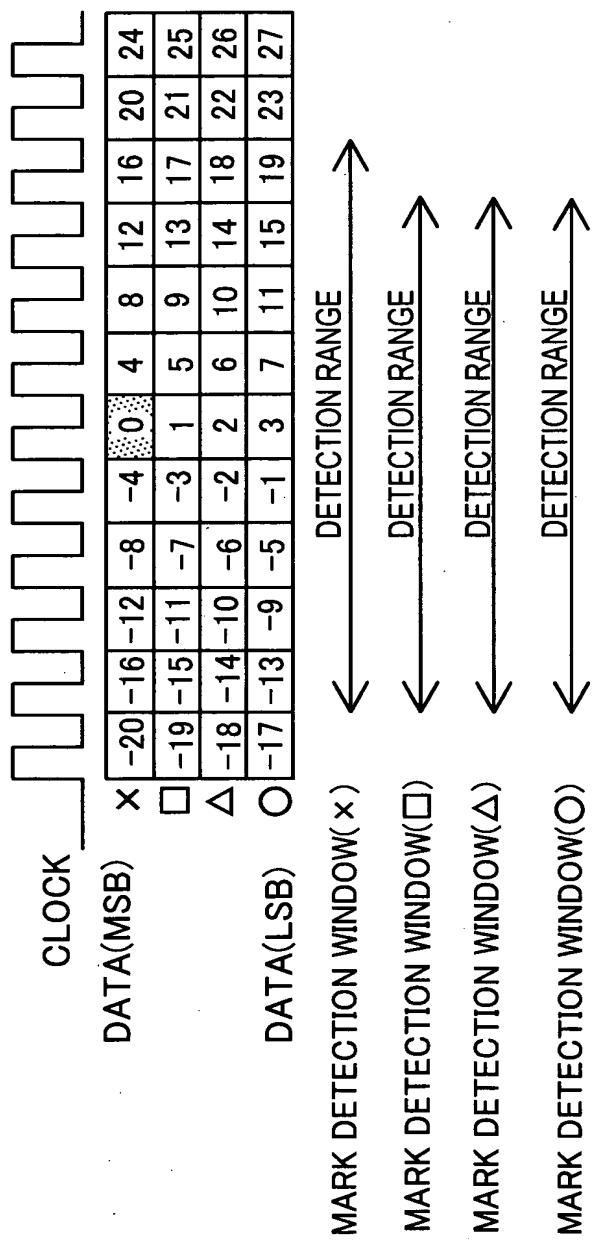


FIG.8

BLOCK DIAGRAM ILLUSTRATING BASIC STRUCTURE OF CONTROLLER UNIT OF DATA PROCESSOR WHEN A DVD - ROM IS USED

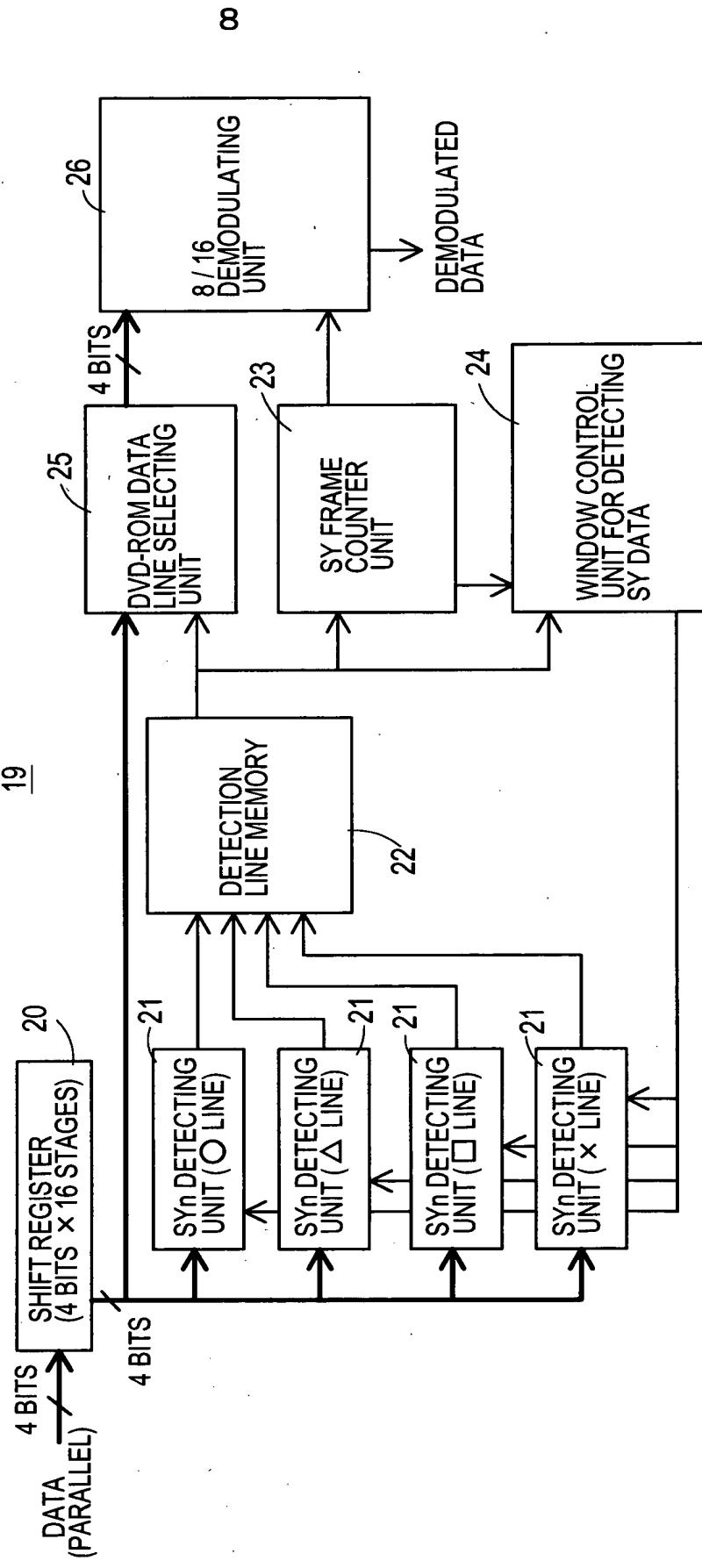


FIG.9

DIAGRAM ILLUSTRATING A DATA FORMAT OF A DVD - ROM IN
DATA PROCESSOR USING THE DVD - ROM

SY0	DATA 91BYTE	SY5	DATA 91BYTE
SY1	DATA 91BYTE	SY5	DATA 91BYTE
SY2	DATA 91BYTE	SY5	DATA 91BYTE
SY3	DATA 91BYTE	SY5	DATA 91BYTE
SY4	DATA 91BYTE	SY5	DATA 91BYTE
SY1	DATA 91BYTE	SY6	DATA 91BYTE
SY2	DATA 91BYTE	SY6	DATA 91BYTE
SY3	DATA 91BYTE	SY6	DATA 91BYTE
SY4	DATA 91BYTE	SY6	DATA 91BYTE
SY1	DATA 91BYTE	SY7	DATA 91BYTE
SY2	DATA 91BYTE	SY7	DATA 91BYTE
SY3	DATA 91BYTE	SY7	DATA 91BYTE
SY4	DATA 91BYTE	SY7	DATA 91BYTE

FIG. 10

BLOCK DIAGRAM ILLUSTRATING BASIC STRUCTURE OF CONTROLLER UNIT OF DATA PROCESSOR WHEN AN MO IS USED

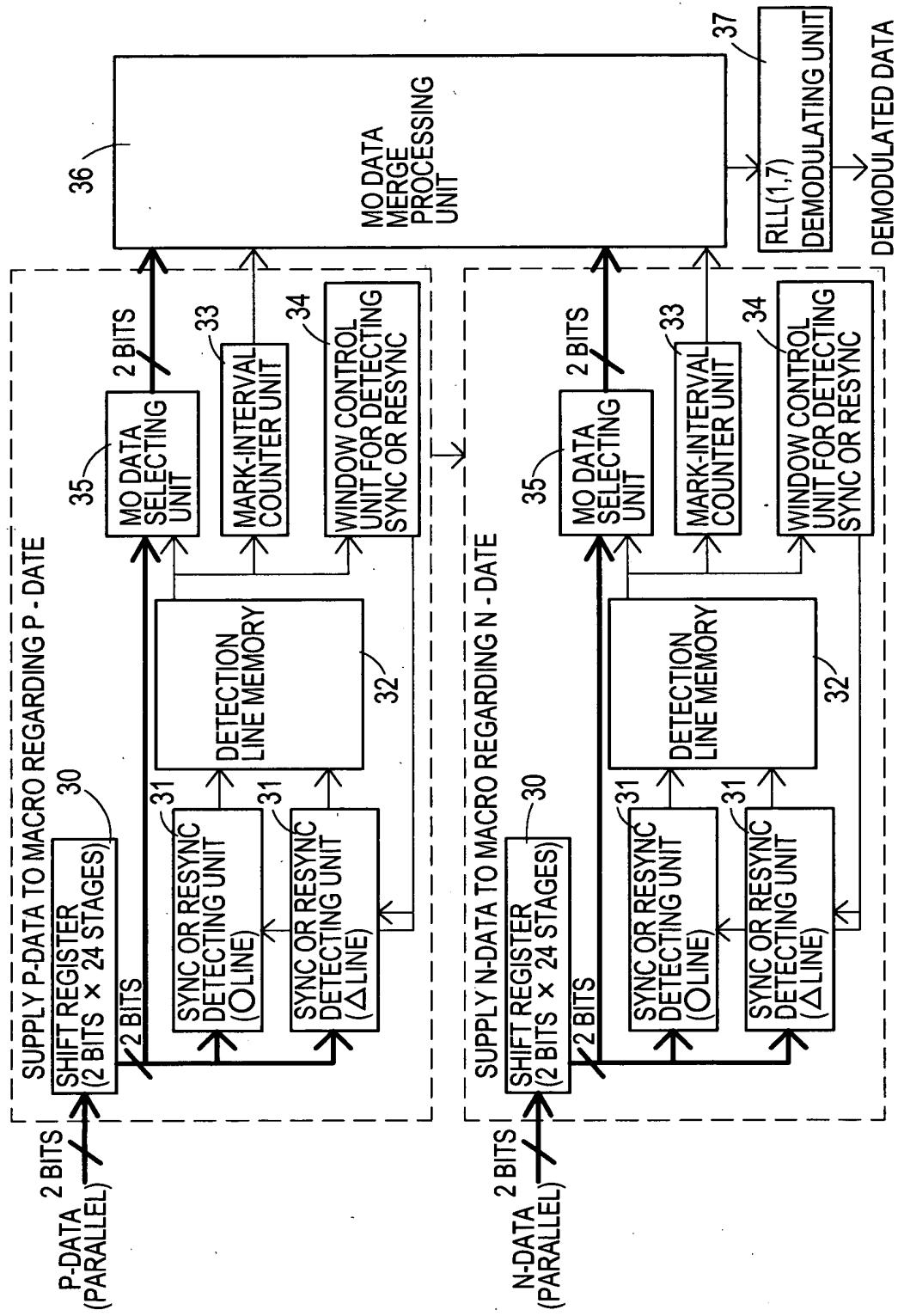


FIG. 11

EXPLANATORY DIAGRAM FOR DISTRIBUTION OF DATA IN PARALLEL CONDITION OF TWO BITS

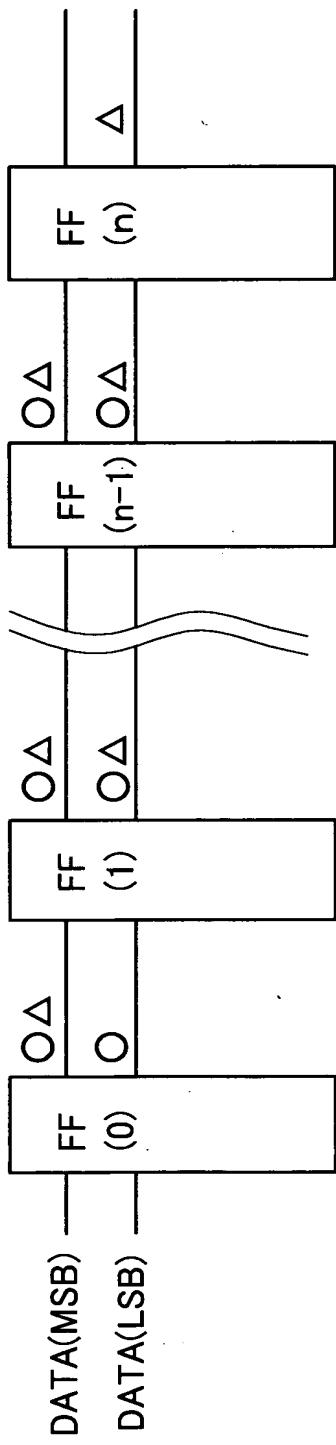


FIG. 12

EXPLANATORY DIAGRAM FOR GENERATION OF MARK DETECTION WINDOW WHEN
PREDETERMINED MARKS FOR DETECTING SYNCHRONIZATION ARE DETECTED IN
O - LINE AT THE TIME OF TRANSFERRING DATA IN PARALLEL CONDITION OF TWO BITS

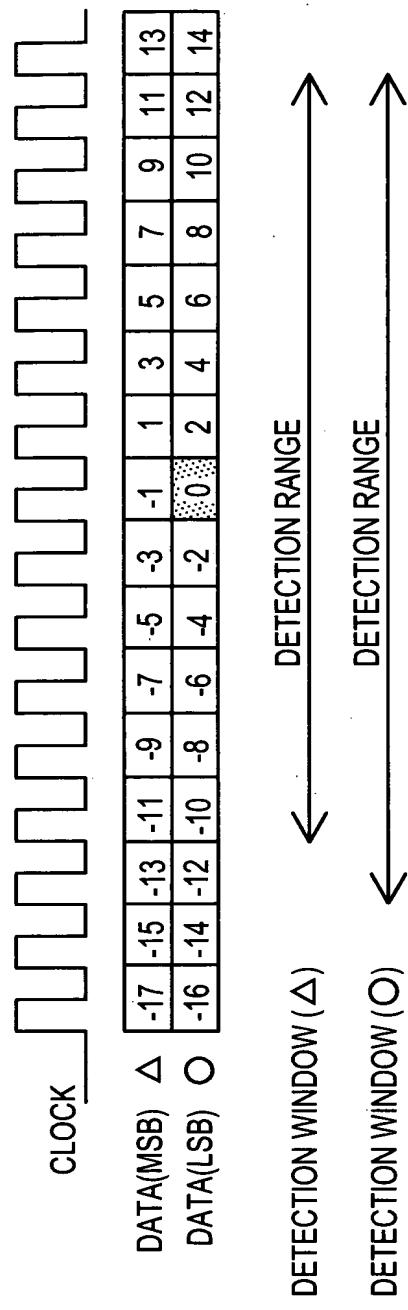


FIG. 13

EXPLANATORY DIAGRAM FOR GENERATION OF MARK DETECTION WINDOW WHEN
PREDETERMINED MARKS FOR DETECTING SYNCHRONIZATION ARE DETECTED IN
 Δ - LINE AT THE TIME OF TRANSFERRING DATA IN PARALLEL CONDITION OF TWO BITS

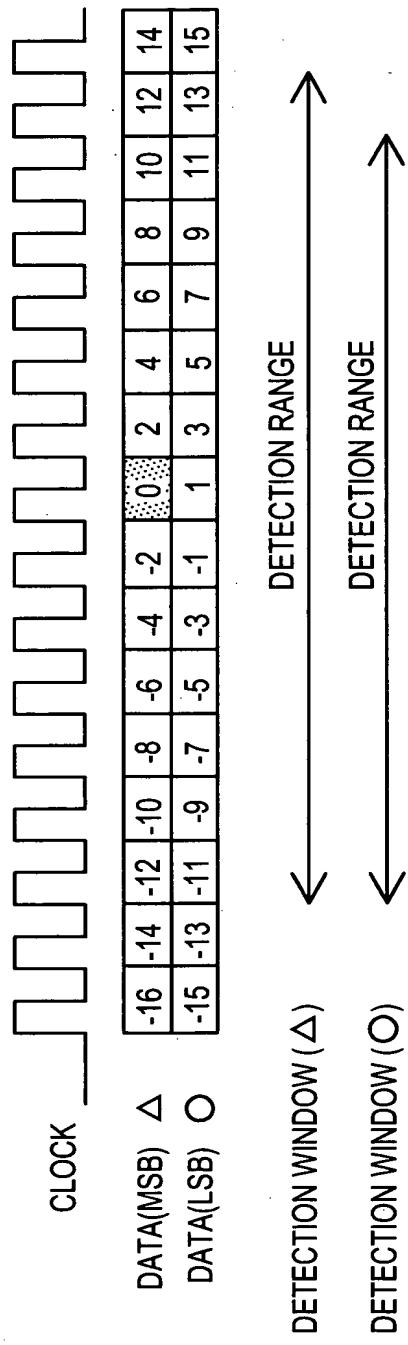


FIG.14

DIAGRAM ILLUSTRATING A DATA FORMAT OF DATA PROCESSOR WHEN AN MO IS USED

FIG. 15
SYSTEM STRUCTURE DIAGRAM ILLUSTRATING THE BASIC STRUCTURE OF
CONTROLLER UNIT OF DATA PROCESSOR OF OTHER EMBODIMENT

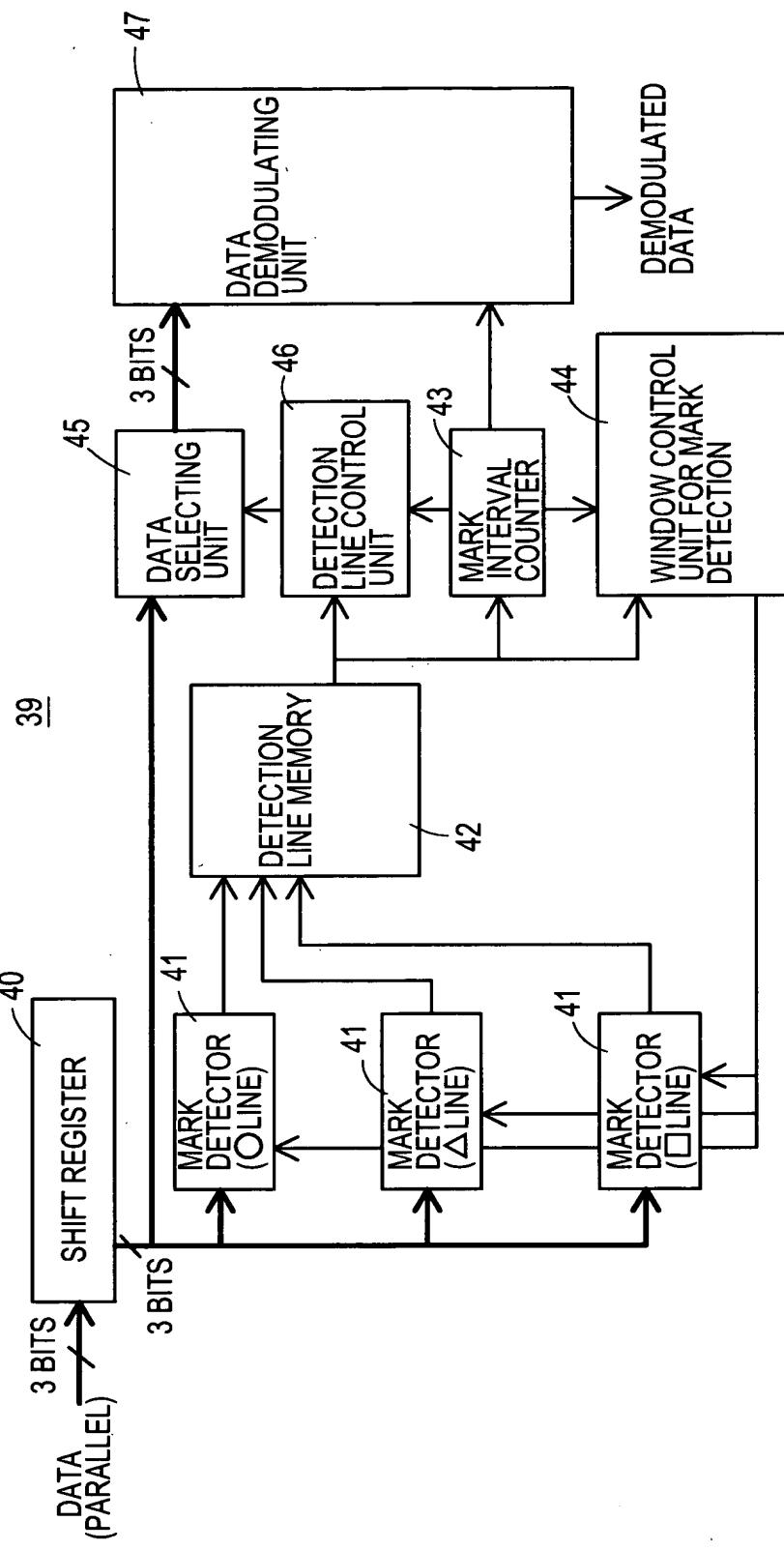


FIG. 16
EXPLANATORY DIAGRAM FOR DISTRIBUTION OF DATA IN PARALLEL CONDITION OF THREE BITS

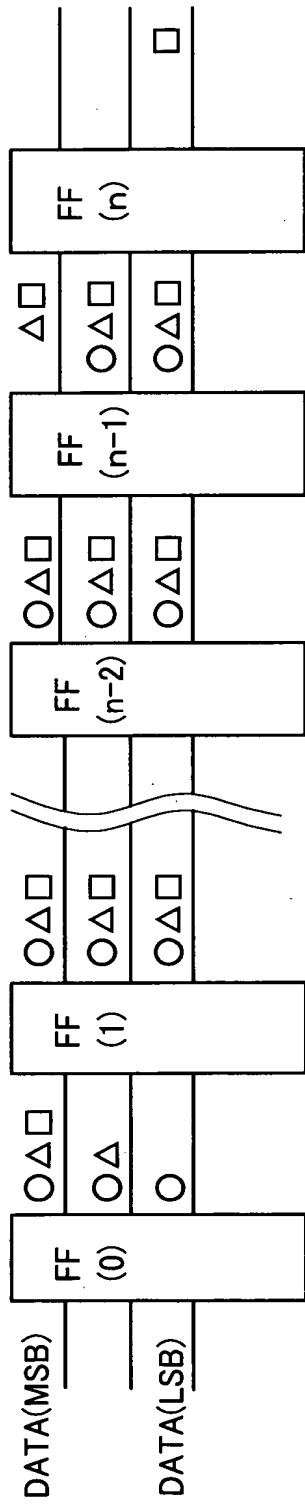


FIG.17 PRIOR ART

STRUCTURAL DIAGRAM ILLUSTRATING DATA PROCESSOR FOR READING DATA FROM A MEMORY MEDIUM OF RELATED ART

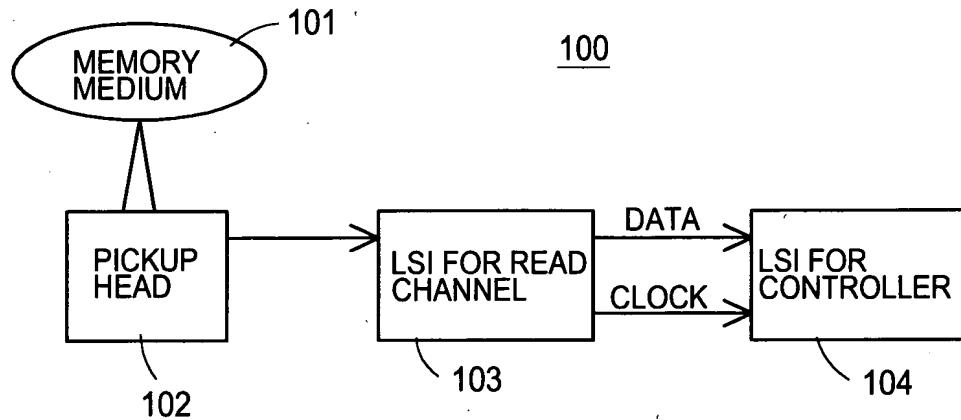


FIG.18 PRIOR ART

DIAGRAM ILLUSTRATING A STRUCTURE IN CONTROLLER OF RELATED ART FOR PROCESSING THE SERIAL DATA TRANSFERRED FROM READ CHANNEL UNIT

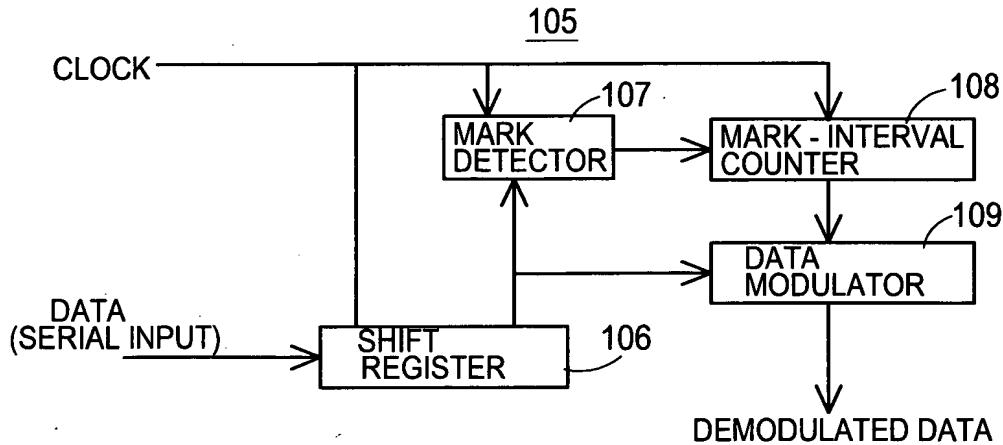


FIG. 19 PRIOR ART

DIAGRAM ILLUSTRATING A STRUCTURE IN CONTROLLER OF RELATED ART (IN PARALLEL CONDITION)

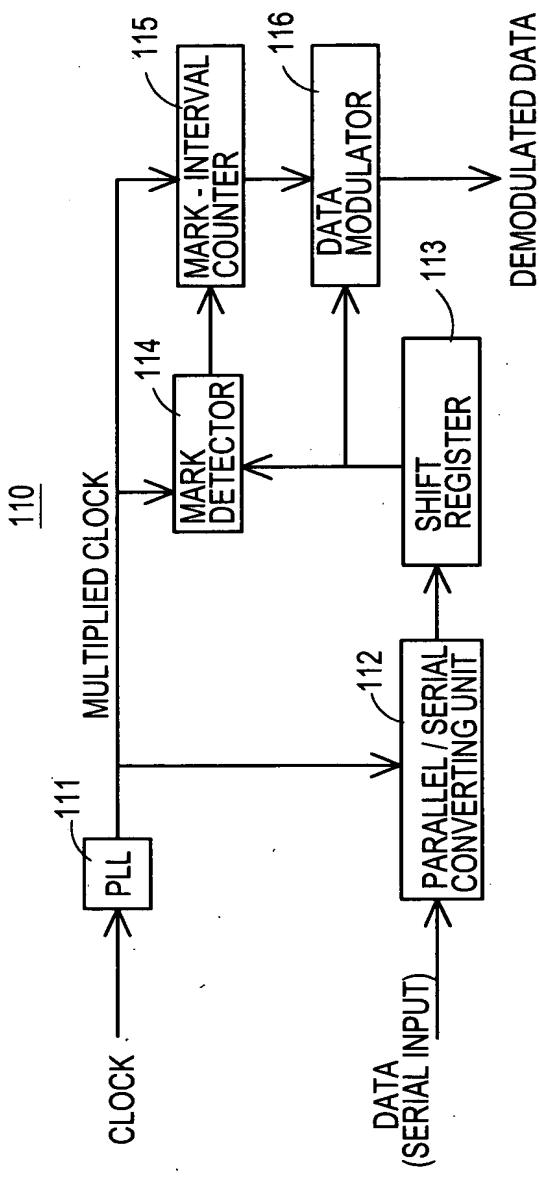


FIG.20

EXPLANATORY DIAGRAM FOR A METHOD TO DETECT A PATTERN OF PREDETERMINED MARKS IN DATA PROCESSOR OF RELATED ART USING A DVD - ROM

